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MAR 08 2007

Application No. 10/620,456
Amendment dated March 8, 2007
Reply to Office Action of December 8, 2007

Docket No.: 4444-0120P

AMENDMENTS TO THE DRAWINGS

Attached hereto are two (2) sheets of corrected drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected drawings incorporate the following drawing changes:

In FIG. 2A, an enabled example of the compare circuit with behavior defined by the truth table of FIG. 2B is provided.

In FIG. 5, the circuit providing X and Y from T0-T3 is amended in accordance with the original disclosure.

FIG.2A and FIG.5 are simply exemplified embodiments for the circuits defined by the truth tables of FIG. 2B and FIG. 6 respectively. It is respectfully submitted that no new matter is present.

It is respectfully requested that the corrected drawings be approved and made a part of the record of the above-identified application.

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REMARKS

Claims 1-18 remain present in the application.

The specification and claims 1-18 have been amended. Reconsideration of the application, as amended, is respectfully requested.

Objection to the Claims

Claim 14 stands objected to for an informality. In view of the foregoing amendments, it is respectfully submitted that this objection has been addressed. Reconsideration and withdrawal of any objection to the claims are respectfully requested.

Rejections under 35 USC 112

Claims 9 and 18 stand rejected under 35 USC 112, first paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, it is respectfully submitted that the claims would enable one of ordinary skill in the art to make and/or use the instant invention. Reconsideration and withdrawal of the 35 USC 112, first paragraph rejection are respectfully requested.

Claims 2-9 and 11-18 stand rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, it is respectfully submitted that all claims particularly point out and distinctly claim the subject matter of the instant invention. Reconsideration and withdrawal of the 35 USC 112, second paragraph rejection are respectfully requested.

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Rejections under 35 USC 102 and 103

Claims 1-5, 7-8, 10-13, 15 and 17 stand rejected under 35 USC 102(b) as being anticipated by Kiso et al, U.S. Patent 5,757,809. This rejection is respectfully traversed.

Claims 6 and 16 stand rejected under 35 USC 103 as being unpatentable over Kiso in view of Roohpavar, U.S. Patent 7,047,45. This rejection is respectfully traversed.

It is respectfully submitted that Kiso fails to anticipate the claimed memory modeling circuit of the present invention.

With regard to claims 1 and 10, the compare circuit is restricted to a feature essential to the fault toleration property. The claimed compare circuit compares the number of 0's and 1's in the input ends and outputs the binary value contained in a majority number of the input ends. Referring to FIG. 2B, for example, if there are two 0's and one 1's in the input ends, then the comparison output will be set to 0 as illustrated by the second, third, and fifth rows of the table of FIG. 2B. On the contrary, the fourth, sixth, and seventh rows show the cases that number of 1's prevails over number of 0's and thus a binary value 1 is output.

The pattern comparing circuit C recited by Kiso fails to anticipate the claimed compare circuit. Specifically, the recited pattern comparing circuit C does not compare "at least three data inputs from different memories, wherein if the data inputs are divided into a first kind data and a second kind data and if the count of the first kind data outnumbered that of the second kind data, the compare circuit will output the first kind data," as is recited in the present application.

It is noted that support for this feature in the claims can be found in the truth table disclosed in FIG. 2B for the compare circuit. Additionally, this feature is supported by the

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specification. For example, page 8, lines 20-24 of the specification set forth that, " the correct output data can be gotten through the compare circuit unless two faults occur simultaneously on the output/input ports DQ0 among the first memory 100, the second memory 102 and the third memory 104." In other words, a memory modeling circuit with the compare circuit according to claim 1 will function properly unless two faults out of three occur simultaneously, or in a more general case, unless most of the memories out of order.

In view of the foregoing amendments and remarks, it is respectfully submitted that the circuit of independent claims 1 and 10 of the present application, as well as their dependent claims, is neither taught nor suggested by the prior art utilized by the Examiner. Reconsideration and withdrawal of the 35 USC 102 rejection are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

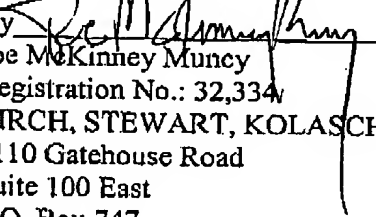
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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: March 8, 2007

Respectfully submitted,

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